## IN THE UNITED STATES PATENT OFFICE

oplicants:

Bernard J. New et al.

Assignee:

Xilinx, Inc.

Title:

"MULTI-SPEED DELAY-LOCKED LOOP"

Serial No.:

10/719,743

File Date:

November 21, 2003

Examiner:

Hai L. Nguyen

Art Unit:

2816

Docket No.: X-1141 US

Conf. No.:

3152

**COMMISSIONER FOR PATENTS** 

P.O. Box 1450

Alexandria, Virginia 22313-1450

## SUBMISSION OF SUBSTITUTE REFERENCE

## Dear Sir:

The enclosed reference was submitted with the application at the time of filing however, the Examiner's written note on Substitute Form PTO-1449A/PT states, "not considered because the document is not provided." Applicants hereby submit a copy of the Substitute Form PTO-1449A/PT, Return Receipt Postcard and a substitute copy of the previously submitted reference.

Applicants believe no fee is due with this communication.

The Commissioner is hereby authorized to charge any additional fees, or credit any overpayment which may be required to Deposit Account No. 24-0040.

Respectfully submitted,

Justin Liu

Attorney for Applicants

Reg. No. 51,959

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450/on February 11. 2005.

Julie Matthews

Name

JL: jam

PTO/SE/08A (10-01)
Approved for use through 10/31/2002. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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VIII O	INFO	RMATION	1 DI	SCLOSURE	Filing Date	November 21, 2003				
	STATEMENT BY APPLICANT				First Named Inventor	Bernard J. New				
	JIA		J.,	AI I LIOAII I	Art Unit	2816				
	(u	se as many she	ets as	necessary)	Examiner Name	Hai L. Nguyen				
	Sheet	1	of	1	Attorney Docket Number	X-1141 US				

		OTHER NON PATENT LITERATURE DOCUMENTS	_
Examiner Initials *	Cite No <sup>.1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		XILINX, INC., "Using Delay-Locked Loops in Spartan-II FPGAs," Application Note: Spartan-II FPGAs, XAPP174, v1.1, January 24, 2000, pp 1-13, Xilinx, Inc., 2100 Logic Drive, San Jose, CA 95124	
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<sup>\*</sup>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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<sup>&#</sup>x27;Applicant's unique citation designation number. 2 Applicant is to place a check mark here if English language Translation is attached.